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MCQs of DLD

1. Which of the following gates give output 1, if and only if at least one input is 1?

A.OR

B.AND

C.NOR

D.NAND

☐ Answer - Click Here:

Α

2. For performing the function of two-input OR gate, What is the minimum number of two-input NAND gates used?

A.2

B.3

C.4

D.5

☐ Answer - Click Here:

В

3. In an application where input signals may ______, Asynchronous circuits are useful.

A. never change

B. change at any time

C. both a and b

D. None

☐ Answer - Click Here:

C

4. The time required by a gate or inverter to change their state is called

lational way

A.Rise time

B.Decay time

C.Charging time

D.Propagation time

☐ Answer - Click Here:

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5. The next state is determined in a sequential circuit is determined by and
A. Current state and external input
B. Current state, flip-flop output
C. State variable, current state
D. Input and clock signal applied
☐ Answer - Click Here:
A
6. SR latch contain
A. 4 input
B. 3 inputs
C. 2 inputs D. 1 inputs
D. 1 mputs
☐ Answer - Click Here:
C
7. If a pulse change from 10% to 90% of its maximum value, the time
required is known as
A.Rise time
B.Operating speed
C.Propagation time
D.Decay time
☐ Answer - Click Here:
A
8. By using two cascading counters, the divide-by-60 counter in digital clock is implemented.
A. Mod-10, Mod-50.
B. Mod-50, Mod-10
C. Mod-6, Mod-10
D. Mod-50, Mod-6
☐ Answer - Click Here:
C
9. Which table is not a part of the asynchronous analysis procedure?
A. transition table
B. excitation table
C. <u>flow table</u>
D. state table

☐ Answer - Click Here:

	data can be applied to <u>gate</u> by maximum frequency which is called
A. Charging	
B. Propagation	
	vel transaction period
D. Operating	speed
☐ Answer - 0	Click Here:
D	
	m time for which input signal maintained at the input of flip-flop is
A. Set-up tin	ne
B. Hold time	
	bility time (PST)
D. Pulse Inte	erval time
☐ Answer - 0	Click Here:
В	
12. For mal	king a <u>transition table</u> we use
A. 3 steps	
B. 5 steps	
C. 6 steps	
D. 8 steps	
☐ Answer - 0	Click Here:
С	
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