Multiple choice of DLD

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**Multiple choices of DLD**

1. __________ is suitable for testing the odd parity of word.
   
   A. AND gate  
   B. OR gate  
   C. NOR gate  
   D. XOR gate

   □ Answer - Click Here:
   
   D

2. Due to change in one input variable, different internal variable change, this makes ____________.
   
   A. Hold delay  
   B. Hold and Wait  
   C. Clock Skew  
   D. Race condition

   □ Answer - Click Here:
   
   D

3. In asynchronous circuit __________ is responsible for occurring changes.
   
   A. clock pulse  
   B. Input  
   C. output  
   D. time

   □ Answer - Click Here:
   
   B

4. ____________ will give the sum of full adders as output.
   
   A. Three-point majority circuit  
   B. Three-bit parity checker  
   C. Three bit counter  
   D. Three-bit comparator

   □ Answer - Click Here:
   
   D

5. Which of the following input overrides other?
   
   A. Asynchronous override synchronous  
   B. Synchronous override asynchronous  
   C. Clear input override Preset Input  
   D. Preset input override Clear input
6. Present state is determined in synchronous circuits by ________________

A. flip-flops  
B. clocked flip-flops  
C. Unlocked flip-flops  
D. latches

7. How many number of full and half-adders required to add 16-bit number?

A. 8 half-adders, 8 full-adders  
B. 16 half-adders, 0 full-adders  
C. 1 half-adder, 15 full-adders  
D. 4 half-adders, 12 full-adders

8. __________ is a decade counter.

A. Mod-10 counter  
B. Mod-5 counter  
C. Mod-8 counter  
D. Mod-3 counter

9. The state of Present and next of asynchronous circuits are also known as __________

A. primary variables  
B. secondary variables  
C. excitation variables  
D. short term memory

10. From maximum value the time required to a pulse to decrease from 90% to 10% is known as ________________.

A. Decay time  
B. Rise time  
C. Binary level transition period  
D. Propagation delay
11. Where is the logic set when the transmission line is idle in the asynchronous transmission?

A. Remains in the previous state  
B. It is set to logic low 
C. It is set to logic high 
D. State of the transmission line is not used to start transmission

☐ Answer - Click Here:

C

12. In ______________ stable state depends on order.

A. defined race 
B. Identical race 
C. non critical race 
D. critical race

☐ Answer - Click Here:

D

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