MCQS

Important MCQs of DLD

By: Prof. Fazal Rehman Shamil Last Modified: April 19, 2020

Important MCQs of DLD

1. Why we use demultiplexer?

- A. Route the data from a single input to one of many outputs
- B. Select data from several inputs and route it to a single output
- C. Perform serial to parallel conversion
- D. Both a and b

\Box	Answer	CI	ick U	loro:
-	Aliswei	- 011	иск п	ere.

D

2. Which is an example of synchronous inputs?

- A. Preset input (PRE)
- B. EN input
- C. J-K input
- D. Clear Input (CLR)

☐ Answer - Click Here:

C

3. Which one is the Second step of making <u>transition table</u>?

- A. determining feedback loop
- B. designating output of loops
- C. deriving functions of Y
- D. plotting

☐ Answer - Click Here:

В

4. We can be imagined that an or gate is look like _____

- A. Switches connected in parallel
- B. Switches connected in series
- C. MOS transistors connected in series
- D. None of these

☐ Answer - Click Here:

Α

5. The change from a current state to the next state is determined by

- A. Previous state and outputs
- B. Current state and outputs
- C. Current state and the inputs
- D. Previous state and inputs

☐ Answer - Click Here:

Search

MCQS

MCQs - Database Systems

MCQs - Computer Network

MCQs Data Structures

MCQs-Computer Science Basics

MCQs - Computer Science

MCQs - English

MCQs - Biology

MCQs - Everyday Science

MCQs – General Knowledge

MCQs – Islamic studies

MCQs - Maths

MCQs - Physics

MCQs - Geography

MCQs - Economics

MCQs - Statistics

MCQs - Programming C Plus

Plus

MCQs - Ethics

MCQs - Visual Programming

MCQs - Management Sciences

MCQs - Social Studies

MCQs - Communication skills

MCQs - General

Engineering MCQs Homepage

Psychology MCQs

Philosophy Of Science

6. Each gate take time for delay
A. 2 to 10 ns
B. 3 to 10 ns
C. 1 to 5 ns
D. 3 to 5 ns
☐ Answer - Click Here:
A
7. In Which combination of gates the arbitrary Boolean function is not possible?
A. OR gates and exclusive OR gate only
B. <u>NAND gates</u> only
C. OR gates and NOT gates only
D. OR gates and AND gates only
☐ Answer - Click Here:
D
8. Which one of the following is used to simplify the circuit that determines the next state?
A. <u>State diagram</u>
B. State assignment
C. State reduction
D. Next state table
☐ Answer - Click Here:
A
9. When both inputs are then NAND latch works.
A. inverted
B. 0
C. 1
D. don't cares
☐ Answer - Click Here:
С
10adders are needed to construct an m-bit parallel adder.
A. m+1
B. m-1
C. m
D. m/2
☐ Answer - Click Here:
В
11 is converted by a multiplexer with a register circuit.
A Sorial data to corial
A. Serial data to serial B. Serial data to parallel

C. Parallel data to serial

D. Parallel da	ta to parallel			
☐ Answer - C	lick Here:			
С				
12. changing in input more than one state is called				
A. undefined B. ideal condi C. reset cond D. <u>race condi</u>	tion ition			
☐ Answer - C	lick Here:			
D				
	Prof. Fazal Rehman Shamil CEO @ T4Tutorials.com I welcome to all of you if you want to discuss about any topic. Researchers, teachers and students are allowed to use the content for non commercial offline purpose. Further, You must use the reference of the website, if you want to use the partial content for research purpose.			

T4Tutorials.com Copvriaht © 2020.

All Copy Rights Reserved By T4Tutorials.com Back to Top ↑